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Serial No.: 09/466,180
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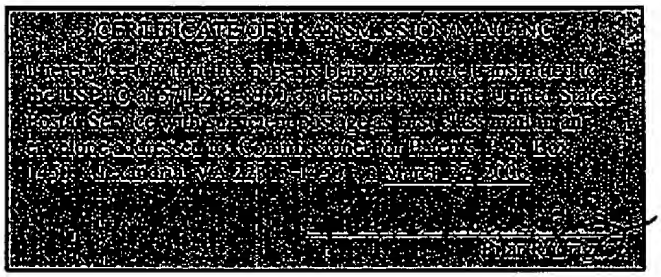
Corporation

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.	:	09/466,180	Confirmation No. 9860
Applicant	:	Donald F. CAMERON et al.	
Filed	:	December 17, 1999	
Title	:	USE OF A TRANSLATION CACHEABLE FLAG FOR PHYSICAL ADDRESS TRANSLATION AND MEMORY PROTECTION IN A HOST	
TC/A.U.	:	2185	
Examiner	:	Denise TRAN	
Customer No.:	:	25693	



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ATTENTION: Board of Patent Appeals and Interferences

APPEAL BRIEF

Dear Sir:

This brief is in furtherance of the Notice of Appeal, filed in this case on December 27, 2005.

1. REAL PARTY IN INTEREST

The real party in interest in this matter is Intel Corporation. (Recorded December 17, 1999, Reel/Frame 010469/0218).

2. RELATED APPEALS AND INTERFERENCES

There are no related appeals.

3. STATUS OF THE CLAIMS

Claims 1, 3-4, 6-12, and 14-30 are pending in the application. Claims 1, 3-4, 6-12, and 14-30 were rejected under 35 U.S.C. §103(a) as being unpatentable over Watkins et al, U.S. Patent No. 5,937,436 (hereinafter "Watkins") in view of Horstmann et al, U.S. Patent No. 6,125,433 (hereinafter "Horstmann"), further in view of Futral et al, U.S. Patent No. 5,991,797 (hereinafter "Futral") and further in view of Garcia et al., U.S. Patent No. 6,163,834 (hereinafter "Garcia").

4. STATUS OF AMENDMENTS

Applicants did not make any amendments to the claim subsequent to final rejection. The claims listed on page 1 of the Appendix attached to this Appeal Brief reflect the present status of the claims (including amendments entered after final rejection).

5. SUMMARY OF THE CLAIMED SUBJECT MATTER

The embodiment of claim 1 generally describes a host coupled to a switched fabric (e.g., page 5, line 8-9 – Figure 1, element 102); including one or more fabric-attached I/O controllers, comprising: a processor (e.g., page 6, line 15 – Figure 2, element 202); a host memory (e.g., page 11, line 3 – Figure 4, element 206) coupled to said processor; and a host-fabric adapter (e.g., page 7, line 5 – Figure 2, element 220) coupled to said processor and provided to interface with said switched fabric, including an internal cache (e.g., page 13, line 7 – Figure 6, element

222) to store selected translation and protection table (TPT) (e.g., page 11, line 1 – Figure 5, element 230) entries from said host memory for a data transaction, each TPT entry comprising protection attributes to control read and write access to a given memory region of said host memory (e.g., page 14, line 5-6 – Figure 7, element 700), a translation cacheable flag to specify whether said host-fabric adapter may flush a corresponding TPT entry (e.g., page 14, line 7 – Figure 7, element 720), a physical page address field to address a physical page frame of data entry (e.g., page 14, line 7 – Figure 7, element 730), and a memory protection tag to specify whether said host-fabric adapter has permission to access said host memory (e.g., page 15, line 20 – Figure 7, element 740); wherein said host-fabric adapter is configured to flush individual cached TPT entries from said internal cache in accordance with the corresponding translation cacheable flag (e.g., page 16, lines 5-7 – Figure 8).

The embodiment of claim 9 generally describes a network, comprising: a switched fabric (e.g., page 5, line 8-9 – Figure 1, element 102); I/O controllers attached to said switched fabric (e.g., page 5, line 10-11 – Figure 1, element 102); and a host comprising an operating system, a host memory (e.g., page 5, line 11 – Figure 1, element 112), and a host-fabric adapter (e.g., page 7, line 5 – Figure 2, element 220) including translation and protection table (TPT) entries, each TPT entry comprising protection attributes to control read and write access to a given memory region of the host memory (e.g., page 11, line 1 – Figure 5, element 230), a translation cacheable flag to specify whether the host-fabric adapter may flush a corresponding TPT entry (e.g., page 14, line 7 – Figure 7, element 720), a physical page address field to address a physical page frame of data entry (e.g., page 14, line 7 – Figure 7, element 730), and a memory protection tag to specify whether the host-fabric adapter has permission to access said host memory (e.g., page 15, line 20 – Figure 7, element 740); wherein the host-fabric adapter is

configured to cache selected TPT entries from the host memory and to flush individual cached TPT entries in accordance with the corresponding translation cacheable flag (e.g., page 16, lines 5-7 – Figure 8).

The embodiment of claim 16 generally describes an apparatus, comprising: a storage device to store translation and protection table (TPT) entries for virtual to physical address translations (e.g., page 11, line 1 – Figure 5, element 230), wherein each of said TPT entries include protection attributes to control read and write access to a given memory region of a host memory (e.g., page 11, line 1 – Figure 5, element 230) and a memory protection tag to specify whether said apparatus has permission to access said host memory (e.g., page 15, line 20 – Figure 7, element 740); and a mechanism to flush individual TPT entries stored in the storage device in accordance with a corresponding translation cacheable flag included in the individual TPT entry (e.g., page 16, lines 5-7 – Figure 8).

The embodiment of claim 21 generally describes a method, comprising: storing, in a cache of an adapter installed in a host system (e.g., page 5, line 11 – Figure 1, element 110) and provided to interface a switched fabric (e.g., page 5, line 8-9 – Figure 1, element 102), translation and protection table (TPT) entries from a host memory for virtual to physical address translations and access validation to the host memory during I/O transactions (e.g., page 11, line 1 – Figure 5, element 230), each of the TPT entries corresponds to a memory portion of the host memory and comprises at least a translation cacheable flag (e.g., page 14, line 7 – Figure 7, element 720) and a memory protection tag to specify whether the adapter has permission to access the host memory(e.g., page 15, line 20 – Figure 7, element 740); and checking a status of the translation cacheable flag of each one or more selected TPT entries stored in the cache of the adapter (e.g., page 15, lines 16-18 – Figure 7) to determine whether to discard one or more

selected TPT entries (e.g., page 15, lines 13-15 – Figure 7) from the cache of the adapter (e.g., page 16, lines 5-7 – Figure 8).

The embodiment of claim 26 generally describes an adapter in a host system provided to interface a switched fabric (e.g., page 5, line 8-9 – Figure 1, element 102), comprising: a cache to store translation and protection table (TPT) entries from a host memory for virtual to physical address translations and access validation to the host memory during I/O transactions (e.g., page 11, line 1 – Figure 5, element 230), each of the TPT entries corresponds to a memory portion of the host memory and comprises at least a translation cacheable flag (e.g., page 14, line 7 – Figure 7, element 720) and a memory protection tag to specify whether the adapter has permission to access the host memory (e.g., page 15, line 20 – Figure 7, element 740); and a mechanism to determine a status of the translation cacheable flag of each one or more selected TPT entries stored in the cache (e.g., page 15, lines 16-18 – Figure 7), and to discard the one or more selected TPT entries from the cache based on the status of the translation cacheable flag (e.g., page 15, lines 13-15 – Figure 7).

FIG. 1 illustrates an example data network according to an embodiment of the present invention;

FIG. 2 illustrates a block diagram of a host of an example data network according to an embodiment of the present invention;

FIG. 3 illustrates a block diagram of a host of an example data network according to another embodiment of the present invention;

FIG. 4 illustrates an example software driver stack of a host of an example data network according to an embodiment of the present invention;

FIG. 5 illustrates an example host-fabric adapter and an example translation and protection table (TPT) of a host of an example data network according to an embodiment of the present invention;

FIG. 6 illustrates an example host-fabric adapter process of flushing all cached translation and protection table (TPT) entries stored in an internal cache during I/0 transactions;

FIG. 7 illustrates an example translation and protection table (TPT) entry which uses a translation cache flag for enabling a host-fabric adapter to advantageously flush or discard only a designated TPT entry in an internal cache according to an embodiment of the present invention;

FIG. 8 illustrates an example host-fabric adapter process of flushing a designated one of cached translation and protection table (TPT) entries using a translation cache flag according to an embodiment of the present invention;

FIGs. 9A and 9B illustrate different examples of VI architecture descriptors;

FIG. 10 illustrates an example send processing technique according to an embodiment of the present invention; and

FIG. 11 illustrates an example write processing technique according to an embodiment of the present invention.

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Are claims 1, 3-4, 6-12, and 14-30 patentable under 35 U.S.C. §103(a) over Watkins in view of Horstmann, further in view of Futral and further in view of Garcia?

7. ARGUMENT

A. Claims 1, 3-4, 6-12, and 14-30 are not obvious under 35 U.S.C. §103(a) over Watkins in view of Horstmann, further in view of Futral and further in view of Garcia.

Applicants respectfully submit that the cited references do not teach, suggest or disclose at least "[a] host coupled to a switched fabric including one or more fabric-attached I/O controllers, comprising: ... a *host-fabric adapter coupled to said processor and provided to interface with said switched fabric*, ... and protection table (TPT) entries from said host memory for a data transaction, each *TPT entry comprising protection attributes to control read and write access to a given memory region of said host memory*, ..., a physical page address field to address a physical page frame of data entry, and *a memory protection tag to specify whether said host-fabric adapter has permission to access said host memory...*" (e.g., as described in claim 1).

I. "...a *host-fabric adapter coupled to said processor and provided to interface with said switched fabric*"

First, Applicants submit that the Watkins reference does not teach, suggest or disclose a "host-fabric adapter" as described in embodiments of the present invention. The Examiner cites to Figure 2A, element 260_K as disclosing a "workstation fabric adapter". Applicants disagree and state that element 260_K is not the equivalent "host-fabric adapter".

Column 3, lines 40-54 of Watkins disclose element 260_K as being a "microprocessor" (e.g., line 41) or an I/O device (e.g., line 48). Applicants submit a standard microprocessor or I/O device is not and the equivalent of a "workstation fabric adapter" as found in embodiments

of the present invention, and is therefore inadequate to serve as the basis of a proper rejection. In order to be a proper §103(a) rejection, the cited references must disclose a "workstation fabric adapter" (as described in claimed embodiments of the present application).

The Garcia, Horstmann and Futral references fail to disclose the relevant limitation as well. Since features of each of the pending claims are not taught or suggested by the cited references, they are insufficient to support a proper §103(a) rejection and reconsideration and reversal of the rejection of claims 1, 3-4, 6-12, and 14-30 under 35 U.S.C. §103(a) is respectfully requested.

II. "...*TPT entry comprising protection attributes to control read and write access to a given memory region of said host memory*"

Next, the Examiner cites column 4, lines 35-50 of Watkins as disclosing "protection attributes to control read and write access to a given memory region of said memory" as described in embodiments of the present application. Applicants disagree. The cited section states:

> A sample physical translation format 281 is also shown in FIG. 2B. In one embodiment, this format 281 includes a valid bit 283, protection bits 285 and the actual physical page bits 287. The valid bit 283, in the descriptor, determines if a specific translation entry will be placed into the ATU (if valid bit 283 is set) or ignored (if valid bit 283 is cleared). *The protection bits 285 are transferred through control line 560 of FIG. 5 in determining whether a page is accessible using the ATU's physical translation for the virtual address.* For instance, a read-only page can be protected from writes with a read only page protection bit. The physical page bits 287 provide the virtual to physical address mapping for the corresponding portion of the data buffer in virtual address space. The data buffer pointed to by the data buffer pointer 273 can span one or more virtual pages and are not necessarily contiguously placed in physical memory (*emphasis supplied).*

Applicants submit that the cited sections do not teach "...protection attributes to control read and write access to a given memory region of said host memory..." as disclosed in the embodiment of claim 1. The protection bits disclosed in Watkins are directed towards the

Watkins ATU or a physical translation unit (see above), *not* towards a memory unit. The Watkins ATU or address translation unit ("ATU"), is described as follows: "an "address translation" is mapping between a virtual address and physical address" (column 1, lines 23-25). Therefore, the protection bits of Watkins are not addressed "*...to control read and write access to a given memory region...*" as disclosed in embodiments of Applicants' invention, but rather directed toward a temporary mapping feature of Watkins. Therefore, the "protection bits" used in the context of an address translation unit as disclosed in Watkins are insufficient to form the basis of a proper 35 U.S.C. §103(a) rejection of independent claim 1.

The Garcia, Horstmann and Futral references fail to make up for the deficiencies of Watkins as well. Since features of each of the pending claims are not taught or suggested by the cited references, they are insufficient to support a proper §103(a) rejection and reconsideration and withdrawal of the rejection of claims 1, 3-4, 6-12, and 14-30 under 35 U.S.C. §103(a) is respectfully requested.

III. "*...a memory protection tag to specify whether said host-fabric adapter has permission to access said host memory...*"

Furthermore, the Examiner asserts that figure 5 and column 4, lines 35-45 of Watkins teaches protection bits are transferred through control lines 560 of Figure 5 while determining whether a page is accessible using the ATU's physical translation for the virtual address and a read only page can be protected from writes with a read-only page protection bit.

Applicants disagree and assert the Watkins reference does not address or describe at all "...a memory protection tag to specify whether said host-fabric adapter has permission *to*

access said host memory" as specifically recited in the embodiment of claim 1. Column 4, lines 35-45 of Watkins

The Office Action cites column 4, lines 35-50 of Watkins as disclosing protection attributes to control read and write access to a given memory region of said memory. The cited section states:

> A sample physical translation format 281 is also shown in FIG. 2B. In one embodiment, this format 281 includes a valid bit 283, protection bits 285 and the actual physical page bits 287. The valid bit 283, in the descriptor, determines if a specific translation entry will be placed into the ATU (if valid bit 283 is set) or ignored (if valid bit 283 is cleared). *The protection bits 285 are transferred through control line 560 of FIG. 5 in determining whether a page is accessible using the ATU's physical translation for the virtual address.* For instance, a read-only page can be protected from writes with a read only page protection bit. The physical page bits 287 provide the virtual to physical address mapping for the corresponding portion of the data buffer in virtual address space. The data buffer pointed to by the data buffer pointer 273 can span one or more virtual pages and are not necessarily contiguously placed in physical memory (*emphasis supplied).*

Applicants submit that the cited sections do not teach "...protection attributes to control read and write access to a given memory region of said host memory..." as disclosed in the embodiment of claim 1. The protection bits disclosed in Watkins are directed towards the Watkins ATU or a physical translation unit (see above), *not* towards a memory unit. The Watkins ATU or address translation unit ("ATU"), is described as follows: "an "address translation" is mapping between a virtual address and physical address" (column 1, lines 23-25). Therefore, the protection bits of Watkins are not addressed "...to control read and write access to a given memory region..." as disclosed in embodiments of Applicants' invention, but rather directed toward a temporary mapping feature of Watkins. The "protection bits" used in the context of a address translation unit as disclosed in Waltkins are insufficient to form the basis of a proper 35 U.S.C. §103(a) rejection of independent claim 1.

Next, the Office Action asserts that figure 5 and column 7, lines 55 and 60-65 of Watkins teaches the physical address outputting under all conditions unless the protection bits

560 signify that the cycle in progress is prohibited due to an attempted write access of a read-only page. Applicants disagree. The cited section states:

> The translated physical address is output from the fifth select element 510 under all conditions unless (i) the CAM.sub.-- Hit line 536 is not asserted thereby indicating a "lookup miss", (ii) the ATU 450 is disabled by System software not asserting an ATU enable line 566, (iii) a cycle status line 568 is not asserted indicating that this particular translation should be avoided, or (iv) the protection bits 560 signify that the cycle in progress is prohibited due to reasons including, but not limited to, an attempted write access of a read-only page.

Applicants submit that the cited sections only further describe the operation of the ATU, but again do not address or describe at all "...a memory protection tag to specify whether said host-fabric adapter has permission *to access said host memory*" as specifically recited in the embodiment of claim 1.

Applicants submit that since Watkins and indeed, none of the cited references disclose "...a memory protection tag to specify whether said host-fabric adapter has permission *to access said host memory*" as specifically recited in the embodiment of claim 1, the §103(a) rejection should be withdrawn.

Next, the Office Action states that Garcia teaches a memory protection tag to specify whether an adapter has permission to access said memory (e.g., fig. 6, tag protection check field, col. 2 lines 20-55). Applicants respectfully disagree and maintain that nowhere in the extensive section cited by the Office Action is the disclosure of a memory protection tag *to specify whether said host fabric adapter has permission to access* a host memory. The reference merely discloses a "protection tag" and states that it is stored in the context memory during the virtual interface creation process.

The Office Action asserts that in column 1, lines 45-55, Garcia teaches that a network interface controller NIC copies data from memory to a network medium and from the medium

to the memory. It further asserts that only memory that has been registered with the NIC and Kernel Agent can be used for data transfers. Lastly it asserts Garcia teaches the NIC has access to the memory protection tags and compares the values to detect invalid accesses of memory. Applicants again maintain regardless of the Office Action's assertions as to the content of these cited sections, none of the cited sections disclose at least a memory protection tag *to specify whether said host fabric adapter has permission to access* a host memory as described in the embodiment of claim 1. Therefore, Applicants further maintain the "protection tag[s]" disclosed in Garcia are again insufficient to form the basis of a proper 35 U.S.C. §103(a) rejection of independent claim 1.

Futral '797 and Horstmann fail to make up for the deficiencies of Garcia and Watkins. Therefore, as shown above, none of at least these argued features are found in the Watkins, Garcia, Futral '797 or Horstmann references taken individually or in combination. Since features of each of the pending claims are not taught or suggested by the cited references, reconsideration and withdrawal of the rejection of claims 1, 3-4, 6-12, and 14-30 under 35 U.S.C. §103(a) is respectfully requested.

Serial No. 09/466,180
Appeal Brief Under 37 CFR 41.37 Filed March 27, 2006
Advisory Action dated January 18, 2006

The Examiner is hereby authorized to charge the appeal brief fee of **$500.00** and any additional fees which may be necessary for consideration of this paper to Kenyon & Kenyon Deposit Account No. **11-0600**.

Respectfully submitted,
KENYON & KENYON LLP

Date: March 27, 2006

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APPENDIX

(Brief of Appellants Donald F. Cameron et al.
U.S. Patent Application Serial No. 09/466,180)

8. CLAIMS ON APPEAL

1. (Previously Presented) A host coupled to a switched fabric including one or more fabric-attached I/O controllers, comprising:

a processor;

a host memory coupled to said processor; and

a host-fabric adapter coupled to said processor and provided to interface with said switched fabric, including an internal cache to store selected translation and protection table (TPT) entries from said host memory for a data transaction, each TPT entry comprising protection attributes to control read and write access to a given memory region of said host memory, a translation cacheable flag to specify whether said host-fabric adapter may flush a corresponding TPT entry, a physical page address field to address a physical page frame of data entry, and a memory protection tag to specify whether said host-fabric adapter has permission to access said host memory;

wherein said host-fabric adapter is configured to flush individual cached TPT entries from said internal cache in accordance with the corresponding translation cacheable flag.

2. (Cancelled)

3. (Previously Presented) The host as claimed in claim 1, wherein each of said selected TPT entries represents translation of a single page of said host memory.

4. (Previously Presented) The host as claimed in claim 1, wherein said host-fabric adapter is provided to perform virtual to physical address translations and validate access to said host memory using said selected TPT entries.

5. (Cancelled)

6. (Previously Presented) The host as claimed in claim 1, wherein said protection attributes comprise a Memory Write Enable flag to indicate whether said host-fabric adapter can write to a page; a RDMA Read Enable flag to indicate whether the page can be a source of a RDMA Read operation; a RDMA Write Enable flag to indicate whether the page can be a target of a RDMA Write operation.

7. (Previously Presented) The host as claimed in claim 1, wherein said host-fabric adapter flushes a designated cached TPT entry from said internal cache when said translation cacheable flag of said designated cached TPT entry indicates a first logical state, and maintains said designated cached translation cacheable flag of said designated cached TPT entry in said internal cache when said translation cacheable flag of said designated cached TPT entry indicates a second logic state opposite of said first logic state.

8. (Previously Presented) The host as claimed in claim 1, further comprising an operating system including driver software which sets status of said translation cacheable flag per TPT entry for enabling said host-fabric adapter to flush individual cached TPT entry from said internal cache.

9. (Previously Presented) A network, comprising:

a switched fabric;

I/O controllers attached to said switched fabric; and

a host comprising an operating system, a host memory, and a host-fabric adapter including translation and protection table (TPT) entries, each TPT entry comprising protection attributes to control read and write access to a given memory region of the host memory, a translation cacheable flag to specify whether the host-fabric adapter may flush a corresponding TPT entry, a physical page address field to address a physical page frame of data entry, and a memory protection tag to specify whether the host-fabric adapter has permission to access said host memory;

wherein the host-fabric adapter is configured to cache selected TPT entries from the host memory and to flush individual cached TPT entries in accordance with the corresponding translation cacheable flag.

10. (Previously Presented) The network as claimed in claim 9, wherein said host-fabric adapter comprises an internal cache to store said selected TPT entries from said host memory.

11. (Previously Presented) The network as claimed in claim 9, wherein each of said selected TPT entries represents translation of a single page of said host memory.

12. (Previously Presented) The network as claimed in claim 9, wherein said host-fabric adapter is provided to perform virtual to physical address translations and validate access to said host memory using said selected TPT entries.

13. (Cancelled)

14. (Previously Presented) The network as claimed in claim 9, wherein said protection attributes comprise a Memory Write Enable flag to indicate whether said host-fabric adapter can write to page; a RDMA Read Enable flag to indicate whether the page can be a source of a RDMA Read operation; a RDMA Write Enable flag to indicate whether the page can be a target of a RDMA Write operation.

15. (Previously Presented) The network as claimed in claim 10, wherein said host-fabric adapter flushes a designated cached TPT entry from said internal cache when said translation cacheable flag of said designated cached TPT entry indicates a first logical state, and maintains said designated cached TPT entry in said internal cache for future re-use when said translation cacheable flag of said designated cached TPT entry indicates a second logic state opposite of said first logic state.

16. (Previously Presented) An apparatus, comprising:

a storage device to store translation and protection table (TPT) entries for virtual to physical address translations, wherein each of said TPT entries include protection attributes to control read and write access to a given memory region of a host memory and a memory protection tag to specify whether said apparatus has permission to access said host memory; and

a mechanism to flush individual TPT entries stored in the storage device in accordance with a corresponding translation cacheable flag included in the individual TPT entry.

17. (Previously Presented) The apparatus as claimed in claim 16, wherein the storage device corresponds to an internal cache for storing said TPT entries.

18. (Previously Presented) The apparatus as claimed in claim 16, wherein each of said TPT entries represents translation of a single page of a host memory.

19. (Previously Presented) The apparatus as claimed in claim 17, wherein each of said TPT entries comprises:

said translation cacheable flag to specify whether said apparatus may flush a corresponding translation and protection table (TPT) entry stored in said internal cache; and

a physical page address field to address a physical page frame of data entry.

20. (Previously Presented) The apparatus as claimed in claim 19, wherein said protection attributes comprise a Memory Write Enable flag to indicate whether said apparatus can write to page; a RDMA Read Enable flag to indicate whether the page can be a source of a RDMA Read operation; a RDMA Write Enable flag to indicate whether the page can be a target of a RDMA Write operation.

21. (Previously Presented) A method, comprising:

storing, in a cache of an adapter installed in a host system and provided to interface a switched fabric, translation and protection table (TPT) entries from a host memory for virtual to physical address translations and access validation to the host memory during I/O transactions, each of the TPT entries corresponds to a memory portion of the host memory and comprises at least a translation cacheable flag and a memory protection tag to specify whether the adapter has permission to access the host memory; and

checking a status of the translation cacheable flag of each one or more selected TPT entries stored in the cache of the adapter to determine whether to discard one or more selected TPT entries from the cache of the adapter.

22. (Previously Presented) The method as claimed in claim 21, further comprising a step of setting the status of the translation cacheable flag per TPT entry, using an operating system (OS), for enabling the adapter to discard individual TPT entries from the cache.

23. (Previously Presented) The method as claimed in claim 21, wherein each of the TPT entries represents translation of a single page of host memory.

24. (Previously Presented) The method as claimed in claim 21, wherein each of the TPT entries comprises:

protection attributes which control read and write access to a given memory region of the host memory;

said translation cacheable flag which specifies whether the adapter may flush a corresponding translation and protection table (TPT) entry stored in the cache; and

a physical page address field which addresses a physical page frame of data entry.

25. (Previously Presented) The method as claimed in claim 21, wherein said protection attributes comprise a Memory Write Enable flag which indicates whether the adapter can write to a page of the host memory; a RDMA Read Enable flag which indicates whether the page can be a source of a RDMA Read operation; a RDMA Write Enable flag which indicates whether the page can be a target of a RDMA Write operation.

26. (Previously Presented) An adapter in a host system provided to interface a switched fabric, comprising:

a cache to store translation and protection table (TPT) entries from a host memory for virtual to physical address translations and access validation to the host memory during I/O transactions, each of the TPT entries corresponds to a memory portion of the host memory and comprises at least a translation cacheable flag and a memory protection tag to specify whether the adapter has permission to access the host memory; and

a mechanism to determine a status of the translation cacheable flag of each one or more selected TPT entries stored in the cache, and to discard the one or more selected TPT entries from the cache based on the status of the translation cacheable flag.

27. (Previously Presented) The adapter as claimed in claim 26, further comprising an operating system (OS) to set the status of the translation cacheable flag per TPT entry for enabling the adapter to discard individual TPT entries from the cache.

28. (Previously Presented) The adapter as claimed in claim 26, wherein each of the TPT entries represents translation of a single page of host memory.

29. (Previously Presented) The adapter as claimed in claim 26, wherein each of the TPT entries comprises:

protection attributes which control read and write access to a given memory region of the host memory;

said translation cacheable flag which specifies whether the adapter may flush a corresponding translation and protection table (TPT) entry stored in the cache; and

a physical page address field which address a physical page frame of data entry.

30. (Previously Presented) The adapter as claimed in claim 26, wherein said protection attributes comprise a Memory Write Enable flag which indicates whether the adapter can write to a page of the host memory; a RDMA Read Enable flag which indicates whether the page can be a source of a RDMA Read operation; a RDMA Write Enable flag which indicates whether the page can be a target of RDMA Write a operation.

9. EVIDENCE APPENDIX

No further evidence has been submitted with this Appeal Brief.

10. RELATED PROCEEDINGS APPENDIX

Per Section 2 above, there are no related proceedings to the present Appeal.